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Amendments to the Claims:

This listing of claims will replace all prior versi n s, and listings, of claims in the application:

Listing of Claims

1 (Currently Amended).    Circuitry for processing images and video, compris ng:

a r ndom access memory;

a motion estimation hardware accele rator coupled to said random access memory;

a transform coding hardware accelera or coupled to said random access memory; and

a processor ~~coupling~~ coupled to said hardware accelerators and to said random access memory for executing software instructions for processing images and video, wherein some of the instructions initiate functions performed by one or more of said hardware accelerators such that the one or more hardware accelerators retrieve data from the random access memory, perform a function on the data, and return a result to the processor.

2 (Original).  The circuitry of claim 1 and further comprising a pixel interpolation hardware accelerator coupled to said random access memory.

3 (Original).  The circuitry of claim 2 wherein said pixel interpolation hardware accelerator performs a half-pixel interpolation function.

4 (Original).  The circuitry of claim 1 wherein said motion estimation hardware accelerator includes circuitry for calculating a mean absolute difference function.

5 (Original).  The circuitry of claim 1 wherein said transform coding hardware accelerator includes circuitry for calculating a direct cosine transform function.

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6 (Original).  The circuitry of claim 5 wherein sai transform coding hardware a c :lerator includes circuitry for calculating an inverse rect cosine transform function.

7 (Currently Amended).    A method of processi ; video information, c r iprising the steps of:

executing a compression task in a programmable rocessing device coupled to a r n dom access memory;

upon encountering a motion estimation instructi ι, initiating execution of an a s )ciated function in a motion estimation hardware ac ·· lerator, said motion estimation h n dware accelerator coupled to said processing device nd said random access m e nory, such that the motion estimation hardware acc ·erator retrieves image data fr ) n the random access memory, performs a motion es nation function on the data, a ic returns a result to the processor; and

upon encountering a transform coding instructic : initiating execution of an a s )ciated function in a transform coding hardware acc ·erator, said transform coding h n dware accelerator coupled to said processing device nd said random access m e nory, such that the transform coding hardware acce rator retrieves image data fr ) n the random access memory, performs a transform · oding function on the data, a ic returns a result to the processor.

8 (Currently Amended).    The method of claim ' step of initiating execution of a i issociated function in the motion estimation hardwa r : accelerator includes the step o: retrieving image data from a data portion of said ran om access memory into said m o ion estimation hardware accelerator.

9 (Currently Amended).    The method of claim ' step of initiating execution of a i issociated function in the transform coding hardwai accelerator includes the step of re trieving image data from a data portion of said rando access memory into said tr n sform coding hardware accelerator.

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10 (Cuɪ  ɪntly Amended).   The method of claim 7 and furthɛ  :omprising the
step of, upon  ɪcountering a pixel interpolation instruction, initiati  execution of an
associated fur  tion in a pixel interpolation hardware accelerator, sɛ  pixel
interpolation :  ɪrdware accelerator coupled to said processing devi.  and said random
access memor  such that the pixel interpolation hardware accelera  r retrieves data
from the rand  ɪn access memory, performs an interpolation functic  on the data, and
returns a resu  to the processor.

11 (Ori  nal). The method of claim 10 wherein said step of in  ating execution of
an associated  ɪnction in a pixel interpolation hardware acceleratoɪ  ɪcludes the step of
performing a  ɪlf-pixel interpolation function.

12 (Ori  nal). The method of claim 7 wherein said step of iniɪ  ting execution of
an associated ɪnction in a motion estimation hardware acceleratoɪ ɪcludes the step of
performing a  ɪean absolute difference function.

13 (Ori  nal). The method of claim 7 wherein said step of iniɪ  ting execution of
an associated  ɪnction in a transform coding hardware accelerator i  ludes the step of
performing a  .rect cosine transform function.

14 (Ori  nal). The method of claim 13 wherein said step of in  ating execution of
an associated  ɪnction in a transform coding hardware accelerator i  ludes the step of
performing aɪ  ɪnverse direct cosine transform function.